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**1 Authoring Support: Automatic detection of 'Goal' segments in basketball videos**

Surya Nepal, Uma Srinivasan, Graham Reynolds

October 2001 **Proceedings of the ninth ACM international conference on Multimedia**

Publisher: ACM Press

Full text available: [pdf \(182.72 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

Advances in the media and entertainment industries, for example streaming audio and digital TV, present new challenges for managing large audio-visual collections. Efficient and effective retrieval from large content collections forms an important component of the business models for content holders and this is driving a need for research in audio-visual search and retrieval. Current content management systems support retrieval using low-level features, such as motion, colour, texture, beat and ...

**Keywords:** content-based retrieval, sports video analysis, temporal models

**2 Efficient dynamic scheduling through tag elimination**



Dan Ernst, Todd Austin

May 2002 **ACM SIGARCH Computer Architecture News , Proceedings of the 29th annual international symposium on Computer architecture ISCA '02 , Proceedings of the 29th annual international symposium on Computer architecture ISCA '02**, Volume 30 Issue 2

Publisher: IEEE Computer Society, ACM Press

Full text available: [pdf \(1.13 MB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#) [Publisher Site](#)

An increasingly large portion of scheduler latency is derived from the monolithic content addressable memory (CAM) arrays accessed during instruction wakeup. The performance of the scheduler can be improved by decreasing the number of tag comparisons necessary to schedule instructions. Using detailed simulation-based analyses, we find that most instructions enter the window with at least one of their input operands already available. By putting these instructions into specialized windows with fe ...

**Keywords:** dynamic scheduling, complexity-effective architecture, low-power architecture, last-tag prediction

**3 Modeling business processes with simulation tools**



Bruce Gladwin, Kerim Tumay

December 1994 **Proceedings of the 26th conference on Winter simulation**

Publisher: Society for Computer Simulation International

Full text available:  pdf(684.42 KB) Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)



#### 4 Power and energy reduction via pipeline balancing

R. Iris Bahar, Srilatha Manne

May 2001 **ACM SIGARCH Computer Architecture News , Proceedings of the 28th annual international symposium on Computer architecture ISCA '01**, Volume 29 Issue 2

Publisher: ACM Press

Full text available:  pdf(1.06 MB) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

*Minimizing power dissipation is an important design requirement for both portable and non-portable systems. In this work, we propose an architectural solution to the power problem that retains performance while reducing power. The technique, known as Pipeline Balancing (PLB), dynamically tunes the resources of a general purpose processor to the needs of the program by monitoring performance within each program. We analyze metrics for triggering PLB, and detail instruction que ...*



#### 5 Superscalar architectures: Select-free instruction scheduling logic

Mary D. Brown, Jared Stark, Yale N. Patt

December 2001 **Proceedings of the 34th annual ACM/IEEE international symposium on Microarchitecture**

Publisher: IEEE Computer Society

Full text available:  pdf(1.00 MB)  Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#)  
[Publisher Site](#)

Pipelining allows processors to exploit parallelism. Unfortunately, critical loops---pieces of logic that must evaluate in a single cycle to meet IPC (Instructions Per Cycle) goals---prevent deeper pipelining. In today's processors, one of these loops is the instruction scheduling (wakeup and select) logic [10]. This paper describes a technique that pipelines this loop by breaking it into two smaller loops: a critical, single-cycle loop for wakeup; and a non-critical, potentially multi-cycle, lo ...



#### 6 Verification of an Industrial CC-NUMA Server

Rajarshi Mukherjee, Yozo Nakayama, Toshiya Mima

January 2002 **Proceedings of the 2002 conference on Asia South Pacific design automation/VLSI Design**

Publisher: IEEE Computer Society

Full text available:  pdf(141.86 KB)  Additional Information: [full citation](#), [abstract](#)  
[Publisher Site](#)

Directed test program-based verification or formal verification methods are usually quite ineffective on large cache-coherent, non-uniform memory access (CC-NUMA) multiprocessors because of the size and complexity of the design and the complexity of the cache-coherence protocol. A controllable biased/constrained random stimuli generator coupled with an error detection mechanism using scoreboards and feedback with coverage analysis tools is a promising alternative methodology. We applied this met ...



#### 7 Innovation management & strategy: The ASpect project case: a model for SME

 adoption of ICT innovation

Piet Boekhoudt, Petra van der Stappen

March 2004 **Proceedings of the 6th international conference on Electronic commerce ICEC '04**

**Publisher:** ACM PressFull text available:  pdf(218.83 KB) Additional Information: [full citation](#), [abstract](#), [references](#)

The process of adoption of technological innovations in Small and Medium sized Enterprises (SMEs) is highly complex. Whereas SMEs are particularly important to the Dutch economy, the innovation potential of SMEs is still highly unused. Information and Communication Technology (ICT) is seen as a modern catalyst for innovation. In this paper we propose the use of a network of SMEs, industry organizations, intermediary parties and knowledge institutes, to achieve adoption of new information and com ...

**Keywords:** SME, application service providing, e-business, innovation, technology adoption

**8 TSEM, a flexible scenario based small forces model** 

Bruce D. Link, Henry D. Shapiro

December 1979 **Proceedings of the 11th conference on Winter simulation - Volume 2****Publisher:** IEEE PressFull text available:  pdf(2.10 MB) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

An accurate computer model of a small force engagement is useful in evaluating the combat effectiveness of armed escorts for sensitive shipments, security guard forces and military patrols. The Transportation Safeguards Effectiveness Model (TSEM), primarily intended for, but not limited to, the study of ambushes of armed convoys, provides the user with considerably greater flexibility in directing the actions of the combatants than previous models. A user oriented script language is present ...

**9 Technical papers: Using transformations to improve semantic matching** 

Peter Z. Yeh, Bruce Porter, Ken Barker

October 2003 **Proceedings of the 2nd international conference on Knowledge capture K-CAP '03****Publisher:** ACM PressFull text available:  pdf(346.72 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

Many AI tasks require determining whether two knowledge representations encode the same knowledge. Solving this *matching problem* is hard because representations may encode the same content but differ substantially in form. Previous approaches to this problem have used either syntactic measures, such as graph edit distance, or semantic knowledge to determine the "distance" between two representations. Although semantic approaches outperform syntactic ones, previous research has focused pri ...

**Keywords:** conceptual graphs, inexact matching, ontology, semantic matching, transformations

**10 Architecture: Virtual multiprocessor: an analyzable, high-performance architecture for real-time computing** 

Ali El-Haj-Mahmoud, Ahmed S. AL-Zawawi, Aravindh Anantaraman, Eric Rotenberg

September 2005 **Proceedings of the 2005 international conference on Compilers, architectures and synthesis for embedded systems CASES '05****Publisher:** ACM PressFull text available:  pdf(376.22 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

The design of a real-time architecture is governed by a trade-off between analyzability necessary for real-time formalism and performance demanded by high-end embedded systems. We reconcile this trade-off with a novel *Real-time Virtual Multiprocessor* (RVMP). RVMP virtualizes a single in-order superscalar processor into multiple interference-free different-sized *virtual processors*. This provides a flexible spatial dimension. In the time dimension, the number and size of virtual proc ...

**Keywords:** hard real-time, resource partitioning, schedulability analysis, simultaneous multithreading, superscalar processor, worst-case execution time

**11 Architecture 2: Using predicate path information in hardware to determine true dependences**

Lori Carter, Brad Calder

June 2002 **Proceedings of the 16th international conference on Supercomputing**

Publisher: ACM Press

Full text available:  pdf(219.76 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

Predicated Execution has been put forth as a method for improving processor performance by removing hard-to-predict branches. As part of the process of turning a set of basic blocks into a predicated region, both paths of a branch are combined into a single path. There can be multiple definitions from disjoint paths that reach a use. Waiting to find out the correct definition that actually reaches the use can cause pipeline stalls. In this paper we examine a hardware optimization that dynamically ...

**Keywords:** dependence analysis, path analysis, predicated execution

**12 Dual Contouring with Topology-Preserving Simplification Using Enhanced Cell Representation**

Nan Zhang, Wei Hong, Arie Kaufman

October 2004 **Proceedings of the conference on Visualization '04**

Publisher: IEEE Computer Society

Full text available:  pdf(588.62 KB) Additional Information: [full citation](#), [abstract](#)

We present a fast, topology-preserving approach for isosurface simplification. The underlying concept behind our approach is to preserve the disconnected surface components in cells during isosurface simplification. We represent isosurface components in a novel representation, called enhanced cell, where each surface component in a cell is represented by a vertex and its connectivity information. A topology-preserving vertex clustering algorithm is applied to build a vertex octree. An enhanced d ...

**Keywords:** isosurface simplification, isosurface extraction, topology preservation, vertex clustering

**13 Posters: Sports video summarization using highlights and play-breaks**

Dian Tjondronegoro, Yi-Ping Phoebe Chen, Binh Pham

November 2003 **Proceedings of the 5th ACM SIGMM international workshop on Multimedia information retrieval**

Publisher: ACM Press

Full text available:  pdf(558.76 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

To manage the massive growth of sport videos, we need to summarize the contents into a more compact and interesting representation. Unlike previous work which summarized either highlights or play scenes, we propose a unified summarization scheme which integrates both highlights and play-break scenes. For automation of the process, combination of audio and visual features provides more accurate detection. We will present fast detection algorithms of whistle and excitement to take advantage of the ...

**Keywords:** content analysis, video summaries

**14 Task and resource allocation via auctioning**

Dharmaraj Veeramani

December 1992 **Proceedings of the 24th conference on Winter simulation****Publisher:** ACM PressFull text available: pdf(925.54 KB) Additional Information: [full citation](#), [references](#), [index terms](#)**15 Talisman: fast and accurate multicomputer simulation**

Robert C. Bedichek

May 1995 **ACM SIGMETRICS Performance Evaluation Review , Proceedings of the 1995 ACM SIGMETRICS joint international conference on Measurement and modeling of computer systems SIGMETRICS '95/PERFORMANCE '95,**

Volume 23 Issue 1

**Publisher:** ACM PressFull text available: pdf(1.24 MB) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

Talisman is a simulator that models the execution semantics and timing of a multicomputer. Talisman is unique in combining high semantic accuracy, high timing accuracy, portability, and good performance. This good performance allows users to run significant programs on large simulated multicomputers. The combination of high accuracy and good performance yields an ideal tool for evaluating architectural trade-offs. Talisman models the semantics of virtual memory, a circuit-switched interno ...

**16 A time-stamping algorithm for efficient performance estimation of superscalar**

processors

Gabriel Loh

June 2001 **ACM SIGMETRICS Performance Evaluation Review , Proceedings of the 2001 ACM SIGMETRICS international conference on Measurement and modeling of computer systems SIGMETRICS '01**, Volume 29 Issue 1**Publisher:** ACM PressFull text available: pdf(1.11 MB) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#)

The increasing complexity of modern superscalar microprocessors makes the evaluation of new designs and techniques much more difficult. Fast and accurate methods for simulating program execution on realistic and hypothetical processor models are of great interest to many computer architects and compiler writers. There are many existing techniques, from profile based runtime estimation to complete cycle-level simulations. Many researchers choose to sacrifice the speed of profiling for the accurac ...

**17 Videoconferencing on the Internet**

Thierry Turletti, Christian Huitema

June 1996 **IEEE/ACM Transactions on Networking (TON)**, Volume 4 Issue 3**Publisher:** IEEE PressFull text available: pdf(1.49 MB) Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#), [review](#)**18 Concept based query expansion**

Yonggang Qiu, Hans-Peter Frei

July 1993 **Proceedings of the 16th annual international ACM SIGIR conference on Research and development in information retrieval****Publisher:** ACM PressFull text available: pdf(1.05 MB) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

Query expansion methods have been studied for a long time - with debatable success in

many instances. In this paper we present a probabilistic query expansion model based on a similarity thesaurus which was constructed automatically. A similarity thesaurus reflects domain knowledge about the particular collection from which it is constructed. We address the two important issues with query expansion: the selection and the weighting of additional search terms. In contrast to earlier methods, ...

**19** [Packet reordering is not pathological network behavior](#) 

Jon C. R. Bennett, Craig Partridge, Nicholas Shectman

December 1999 **IEEE/ACM Transactions on Networking (TON)**, Volume 7 Issue 6

Publisher: IEEE Press

Full text available:  pdf(107.65 KB) Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)

**Keywords:** Internet, communication system traffic, packet switching

**20** [Efficient management of memory hierarchies in embedded DRAM systems](#) 

 Ashley Sausbury, Su-Jaen Huang, Fredrik Dahlgren

May 1999 **Proceedings of the 13th international conference on Supercomputing**

Publisher: ACM Press

Full text available:  pdf(1.57 MB) Additional Information: [full citation](#), [references](#), [index terms](#)

**Keywords:** COMA, DRAM, cache, latency, memory hierarchy, processor

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